IN THE CLAIMS

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims:

1. (Currently Amended) A processor comprising:

a feature indicator associated with at least one of a first sequence of one or more instructions;

a first register;

a second register; and

an execution core;

wherein the feature indicator indicates whether the execution core supports the at least one of the first sequence of one or more instructions, wherein the execution core is configured to execute a first instruction to cause the first register to be set to a first value using the feature indicator and to cause the second register to be set to a second value using the feature indicator, wherein the execution core is configured to execute the first sequence of one or more instructions to cause a function to be performed in response to the first value in the first register indicating a true condition, and wherein the execution core is configured to execute a second sequence of one or more instructions to cause the function to be performed in response to the second value in the second register indicating the true condition.

2. (Original) The processor of claim 1 wherein the execution core is configured to execute the first sequence of instructions as no-operations (NOPs) in response to the first value in the first register indicating a false condition, and wherein the execution core is configured to execute the second sequence of instructions as NOPs in response to the second value in the second register indicating the false condition.

3. (Original) The processor of claim 1 wherein the first instruction comprises a predicate-producing instruction.

4. (Currently Amended) The processor of claim 1 wherein the first instruction comprises a feature specifier associated with at least one of the first sequence of one or more instructions.

5. (Original) The processor of claim 1 wherein the first register comprises a first predicate register and wherein the second register comprises a second predicate register.

6. (Original) The processor of claim 1 wherein the second value is a complement of the first value.

7. (Original) The processor of claim 1 wherein the feature indicator comprises a bit in a features register.

8. (Currently Amended) The processor of claim 1 wherein at least a portion of the first instruction comprises an encoding equivalent to ~~at least a portion of~~ a test NaT instruction that specifies a NaT0 from an Itanium® family instruction set architecture.

9. (Original) The processor of claim 1 wherein the execution core is configured to execute a set of instructions from an Itanium® family instruction set architecture.

10. (Currently Amended) A computer system comprising:

a processor that includes first and second predicate registers and a feature indicator that indicates whether the processor supports at least one of a first sequence of one or more instructions; and

a memory that includes a code segment that is executable by the processor;

wherein the code segment comprises:

a first instruction configured to cause the first and second predicate registers to be set to first and second values, respectively, according to a third value of the feature indicator;

~~a~~ the first sequence of one or more instructions configured to cause a function to be performed in response to the first value in the first predicate register representing a first condition; and

a second sequence of one or more instructions configured to cause the function to be performed in response to the second value in the second predicate register representing the first condition.

11. (Original) The computer system of claim 10 wherein the first sequence of instructions is configured to not cause the function to be performed in response to the first value in the first predicate register representing a second condition, and wherein the second sequence of instructions is configured to not cause the function to be performed in response to the second value in the second predicate register representing the second condition.

12. (Original) The computer system of claim 11 wherein the first condition is true, and wherein the second condition is false.

13. (Canceled)

14. (Canceled)

15. (Currently Amended) The computer system of claim ~~13~~1 wherein the first instruction is configured to cause the first predicate register to be set to the third value, and wherein the first instruction is configured to cause the second predicate register to be set to a complement of the third value.

16. (Currently Amended) The computer system of claim 10 wherein the processor comprises a general purpose register and a bit associated with the general purpose register,

and wherein the first instruction is configured to cause the first and second predicate registers to be set to the first and second values, respectively, according to the bit associated with the general purpose register in response to the processor not supporting the at least one of the first sequence of one or more instructions.

17. (Currently Amended) The computer system of claim 16 wherein the first instruction is configured to cause the first predicate register to be set to ~~the~~ a third value of the bit, and wherein the first instruction is configured to cause the second predicate register to be set to a complement of the third value.

18. (Currently Amended) A method for performing a function in a processor comprising:

setting a first predicate register of the processor to a first value according to a bit in a features register that indicates whether the processor supports at least one of a first sequence of one or more instructions in response to executing a first instruction that includes a feature specifier that identifies the bit;

setting a second predicate register of the processor to a second value according to the bit in response to executing the first instruction;

executing ~~a~~ the first sequence of one or more instructions to perform the function in response to the first value in the first predicate register indicating a true condition; and

executing a second sequence of one or more instructions to perform the function in response to the second value in the second predicate register indicating the true condition.

19. (Canceled)

20. (Original) The method of claim 18 further comprising:

executing the first sequence of instructions as no-operations (NOPs) in response to the first value in the first predicate register indicating a false condition; and

executing the second sequence of instructions as NOPs in response to the second value in the second predicate register indicating the false condition.

21. (Canceled)

22. (Canceled)

23. (Currently Amended) A computer-readable media storing a program executable by a ~~computer system~~processor to cause the ~~computer system~~ processor to:

insert a first instruction into a code segment, the first instruction configured to cause first and second predicate registers to be set to first and second values, respectively, according to a feature indicator in the processor that indicates whether the processor supports at least one of a first sequence of one or more instructions;

insert ~~a~~ the first sequence of one or more instructions into the code segment subsequent to the first instruction, the first sequence of instructions configured to cause a function to be performed in response to the first value indicating a true condition; and

insert a second sequence of one or more instructions into the code segment subsequent to the first instruction, the second sequence of instructions configured to cause the function to be performed in response to the second value indicating a true condition.

24. (Canceled)

25. (Currently Amended) The computer-readable media of claim 23 wherein the first instruction is configured to cause first and second predicate registers to be set to first and second values, respectively, ~~in response~~according to a bit associated with a general purpose register in response to the whether the processor not supporting the at least one of the first sequence of one or more instructions.

26. (Original) The computer-readable media of claim 23 wherein the first sequence of instructions is configured not to cause the function to be performed in response to the first value indicating a false condition.

27. (Original) The computer-readable media of claim 23 wherein the second sequence of instructions is configured not to cause the function to be performed in response to the second value indicating a false condition.

28. (Currently Amended) A processor comprising:

a feature indicator ~~associated with~~that indicates whether the processor supports at least one of a first sequence of one or more instructions;

a predicate register; and

an execution core;

wherein the execution core is configured to execute a predicate-producing instruction to cause the predicate register to be set to a value using the feature indicator, and wherein the execution core is configured to execute a branch instruction to cause the execution core to execute either the first sequence of instructions to perform a function in response to the value indicating a first condition or a second sequence of one or more instructions to perform the function in response to the value indicating a second condition.

29. (Original) The processor of claim 28 wherein the first condition comprises a true condition, and wherein the second condition comprises a false condition.

30. (Original) The processor of claim 28 wherein the first condition comprises a false condition, and wherein the second condition comprises a true condition.

31. (Original) The processor of claim 28 wherein the execution core is configured to execute the branch instruction to cause a branch to be either taken or not taken in response to the value, and wherein the execution core is configured to execute the first sequence of instructions to perform the function in response to the branch being taken.

32. (Original) The processor of claim 28 wherein the execution core is configured to execute the branch instruction to cause a branch to be either taken or not taken in response to

the value, and wherein the execution core is configured to execute the second sequence of instructions to perform the function in response to the branch being taken.